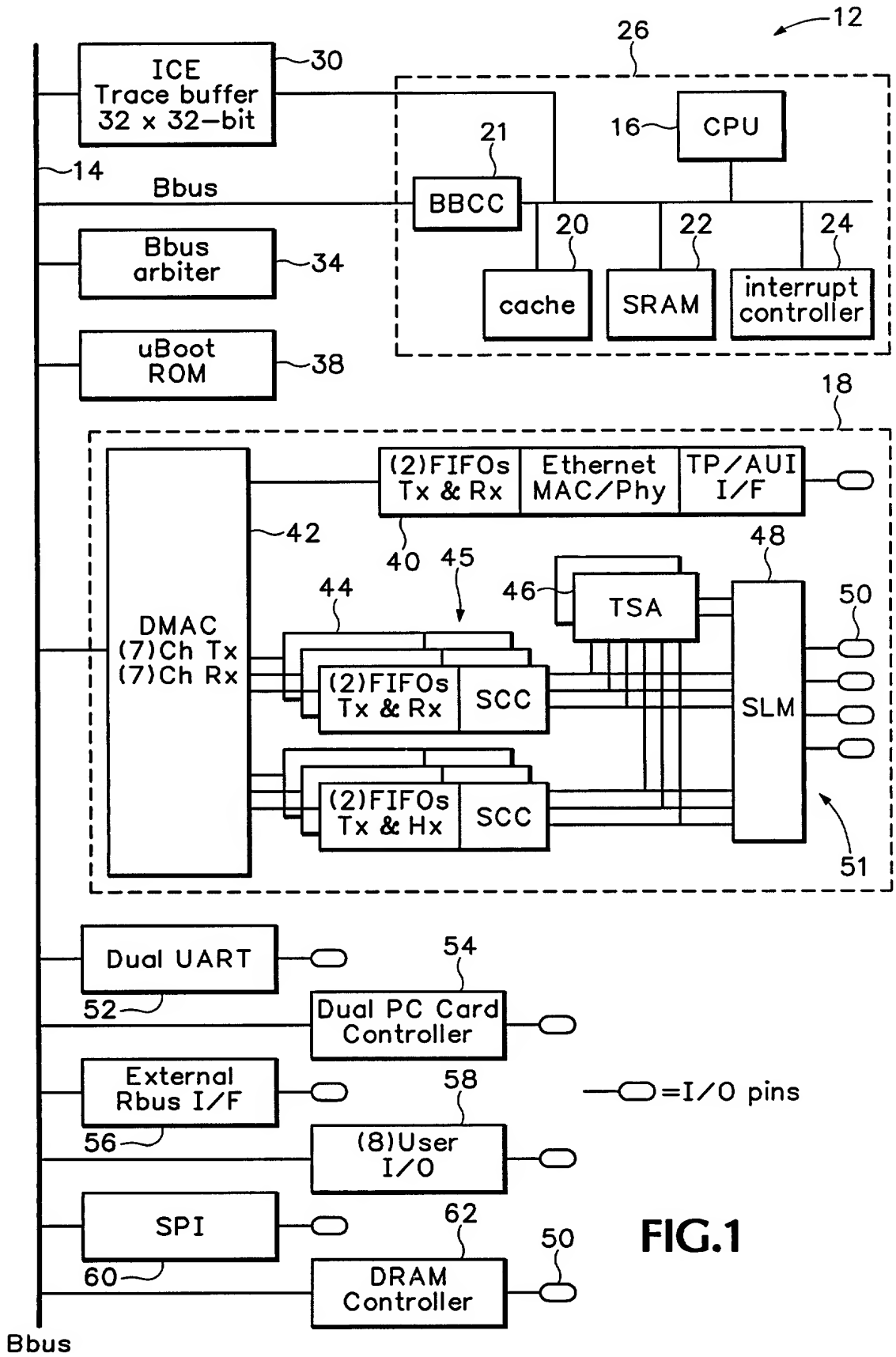
12
26
ICE
Trace buffer
32 x 32-bit
30
21
16
CPU
14
Bbus
BBCC
20
22
24
Bbus
arbiter
34
cache
SRAM
interrupt
controller
uBoot
ROM
38
18
(2)FIFOs
Tx & Rx
Ethernet
MAC/Phy
TP/AUI
I/F
42
40
45
48
44
46
TSA
50
DMAC
(7)Ch Tx
(7)Ch Rx
(2)FIFOs
Tx & Rx
SCC
SLM
(2)FIFOs
Tx & Hx
SCC
51
Dual UART
54
52
Dual PC Card
Controller
External
Rbus I/F
58
=I/O pins
56
(8)User
I/O
SPI
62
50
60
DRAM
Controller
Bbus

FIG.1

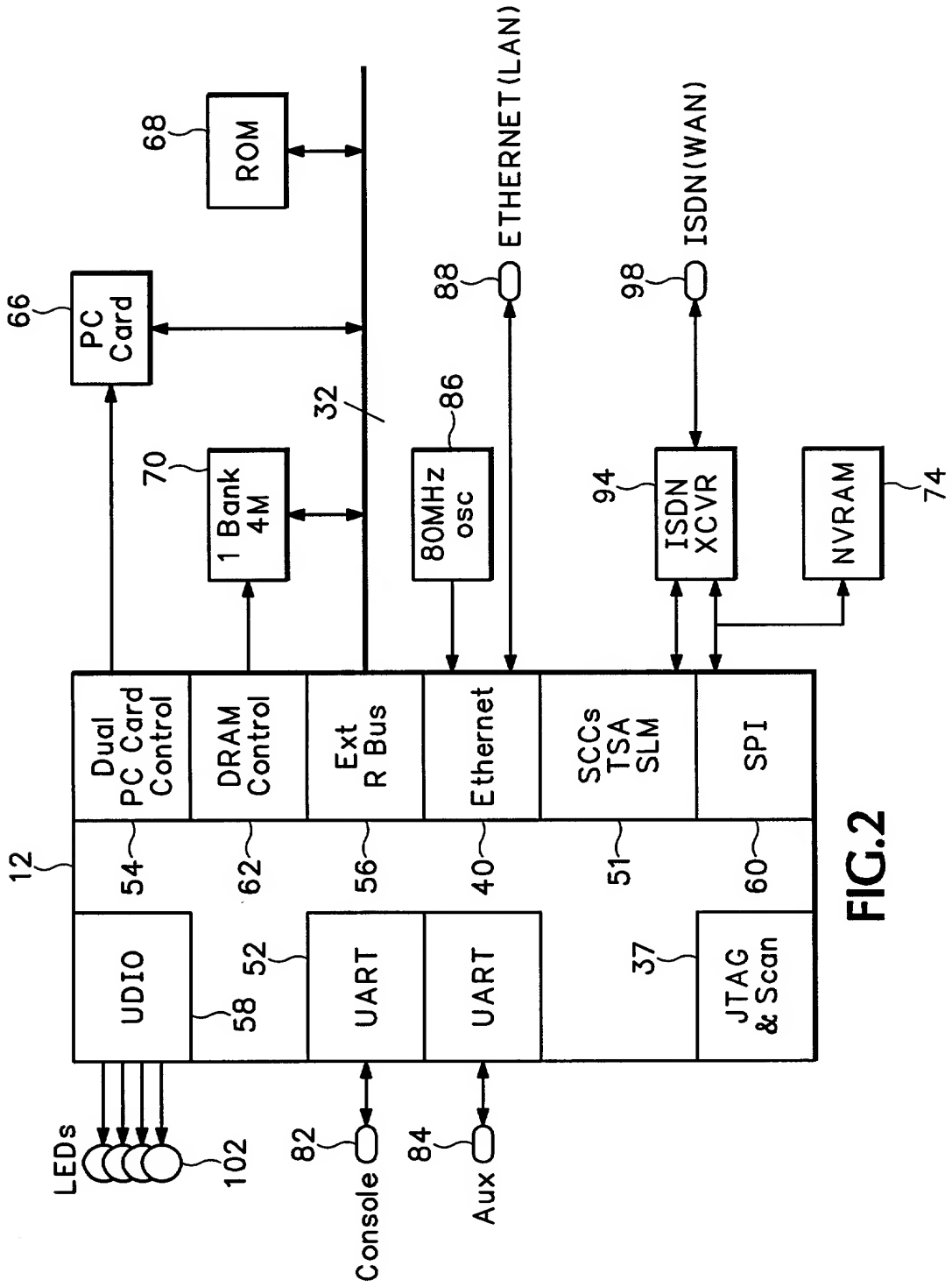
ROM
68
PC Card
66
1 Bank 4M
70
32
80MHz osc
86
ETHERNET (LAN)
88
ISDN (WAN)
98
ISDN XCVR
94
NVRAM
74
Dual PC Card Control
DRAM Control
Ext R Bus
Ethernet
SCCs TSA SLM
SPI
12
54
62
56
40
51
60
UDIO
58
52
UART
UART
37
JTAG & Scan
LEDs
102
82
Console
84
Aux

FIG.2

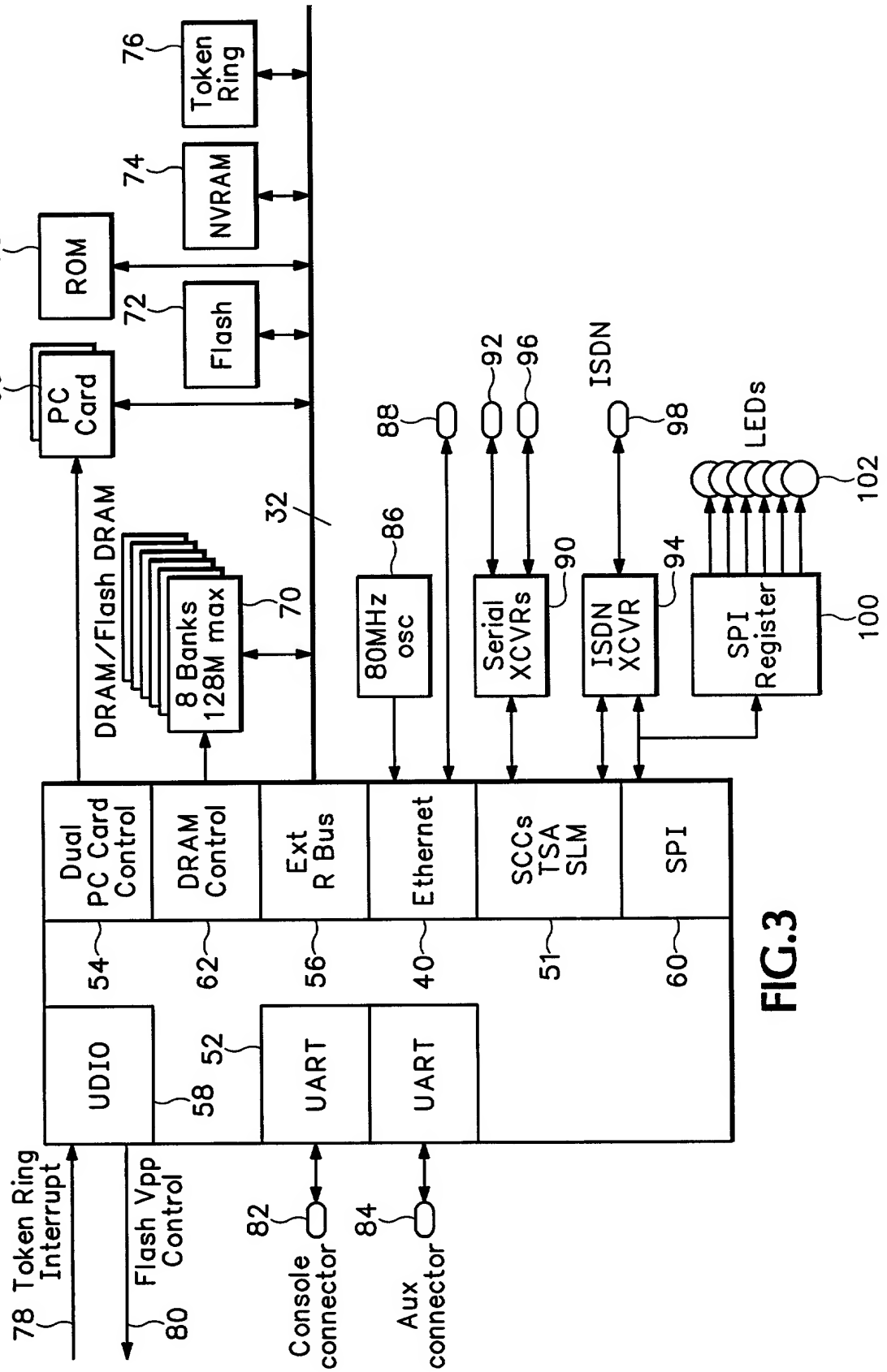
Token Ring
76
NVRAM
74
ROM
68
Flash
72
PC Card
66
DRAM/Flash DRAM
8 Banks 128M max
70
32
80MHz osc
86
88
Serial XCVRs
90
92
96
ISDN XCVR
94
ISDN
98
SPI Register
100
LEDs
102
Dual PC Card Control
DRAM Control
Ext R Bus
Ethernet
SCCs TSA SLM
SPI
54
62
56
40
51
60
UDIO
58
52
UART
UART
78 Token Ring Interrupt
80 Flash Vpp Control
82 Console connector
84 Aux connector

FIG.3

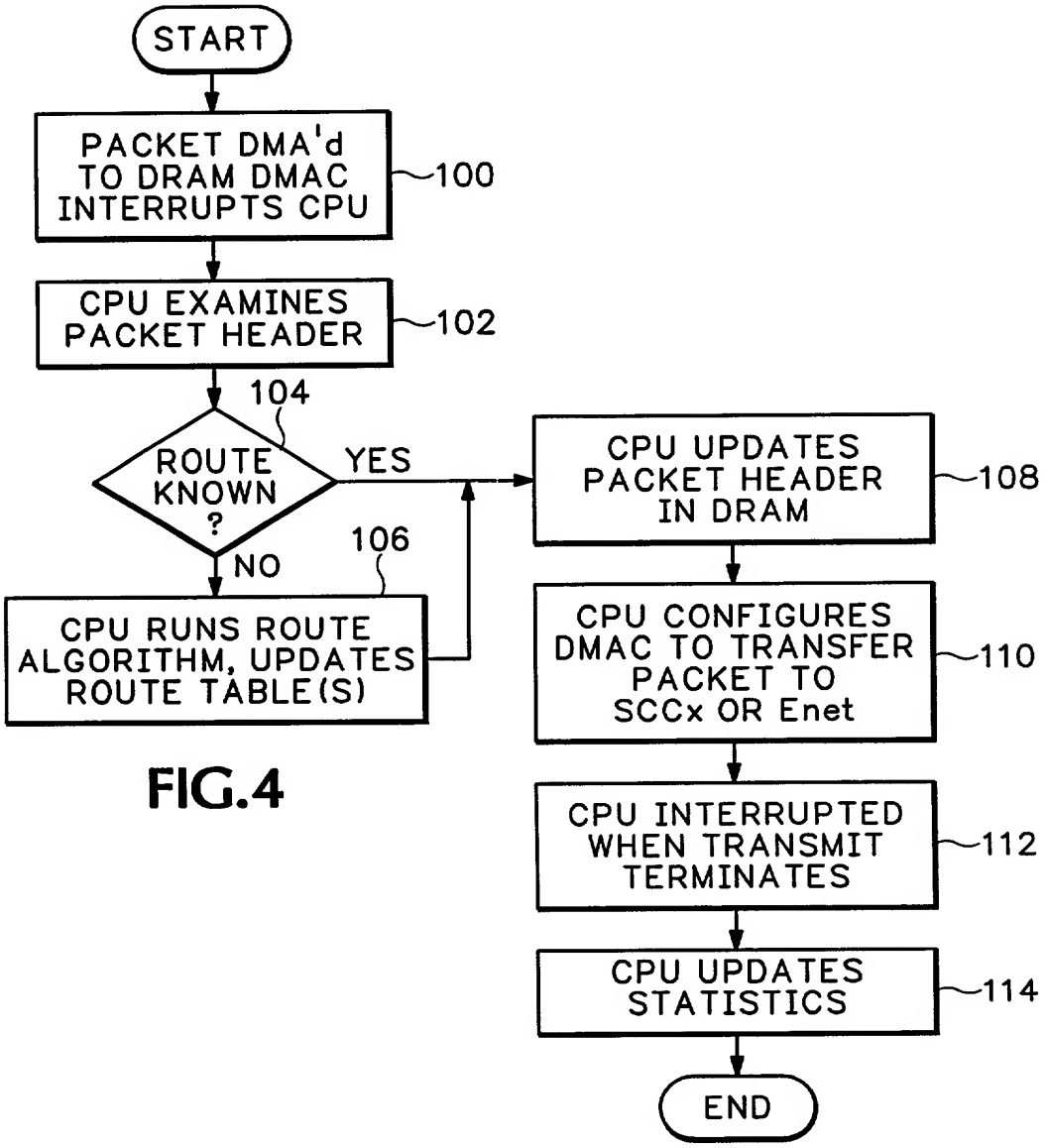
START
PACKET DMA'd TO DRAM DMAC INTERRUPTS CPU
100
CPU EXAMINES PACKET HEADER
102
104
ROUTE KNOWN ?
YES
NO
106
CPU RUNS ROUTE ALGORITHM, UPDATES ROUTE TABLE(S)
CPU UPDATES PACKET HEADER IN DRAM
108
CPU CONFIGURES DMAC TO TRANSFER PACKET TO SCCx OR Enet
110
CPU INTERRUPTED WHEN TRANSMIT TERMINATES
112
CPU UPDATES STATISTICS
114
END

FIG.4

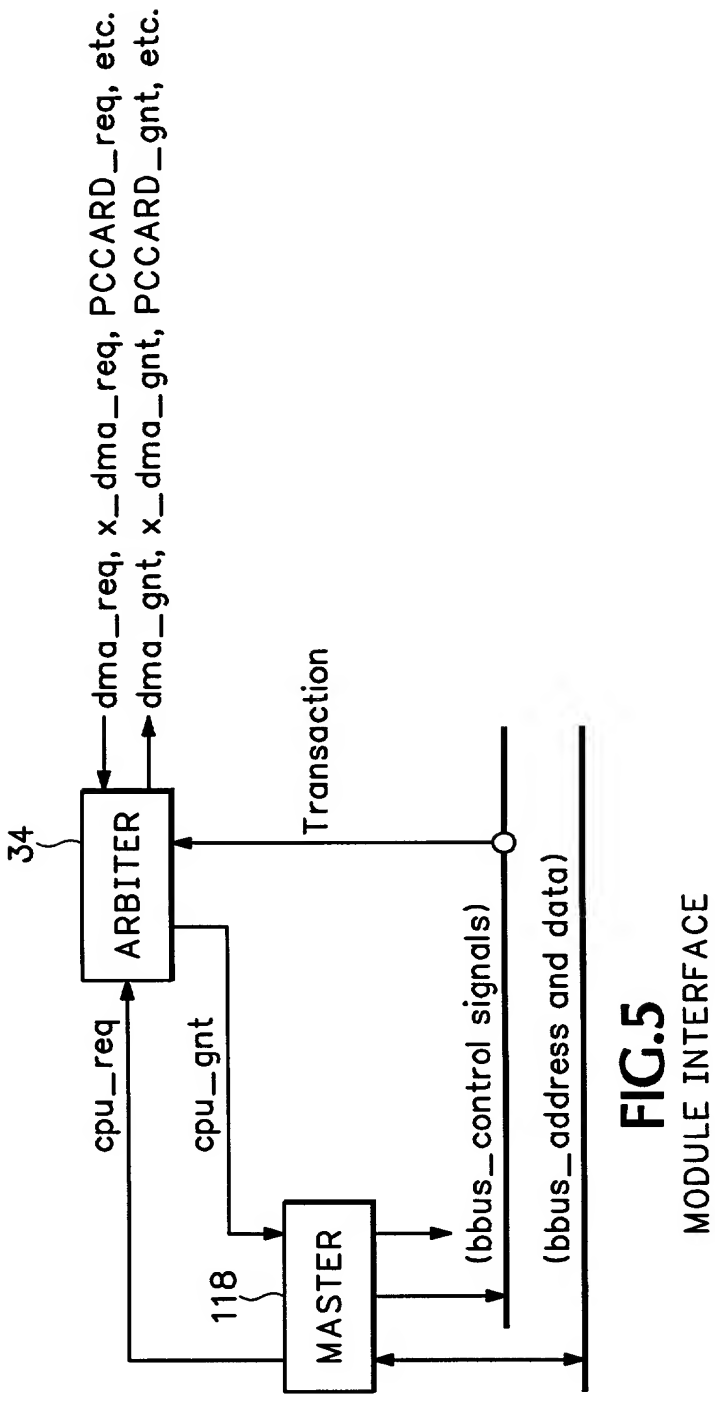

FIG.5
MODULE INTERFACE

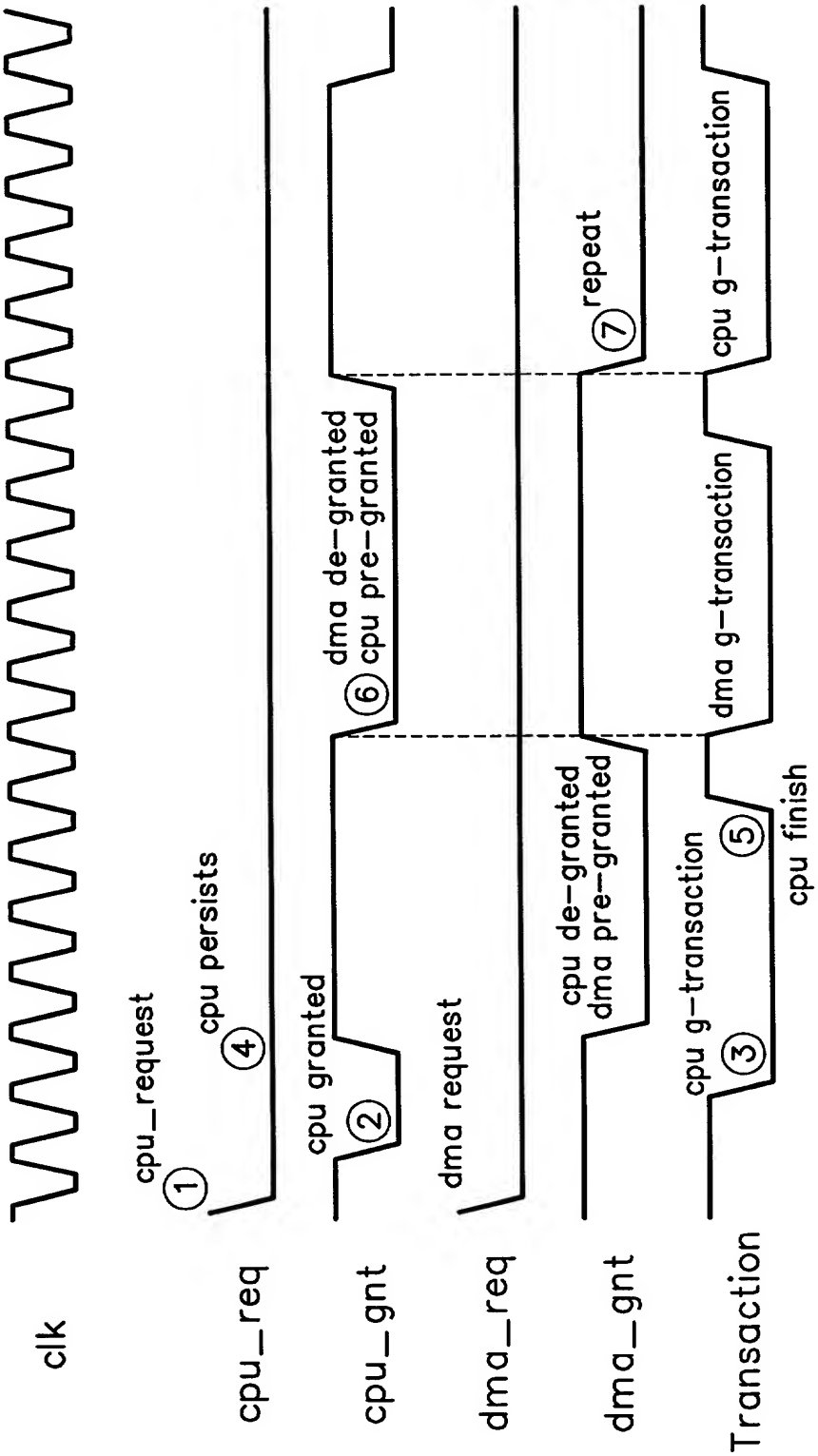

FIG.6
PIPELINED ARBITRATION
PROTOCOL EXAMPLE

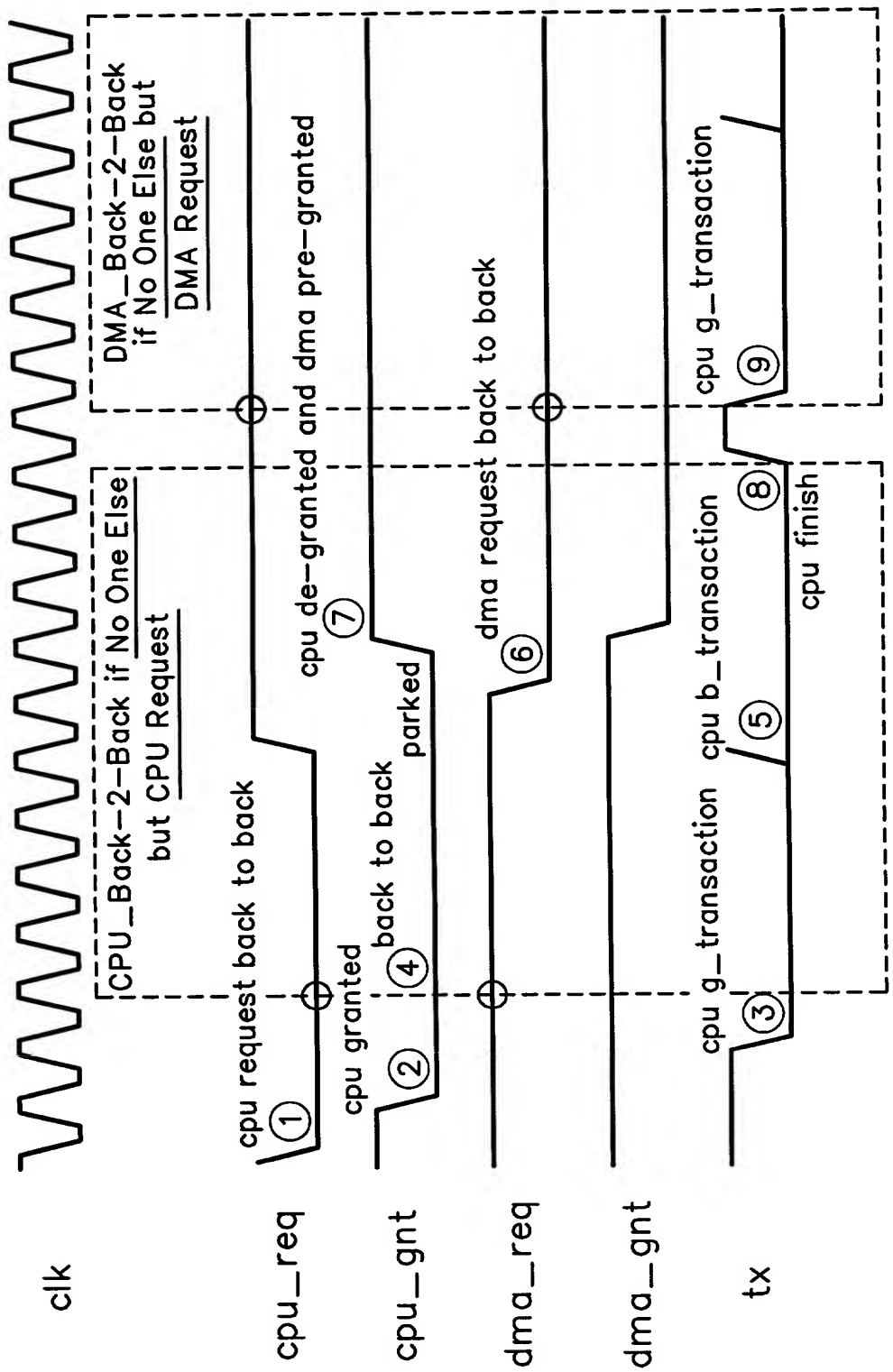

FIG.7
ARBITRATION PROTOCOL EXAMPLE
BACK-TO-BACK TRANSACTION

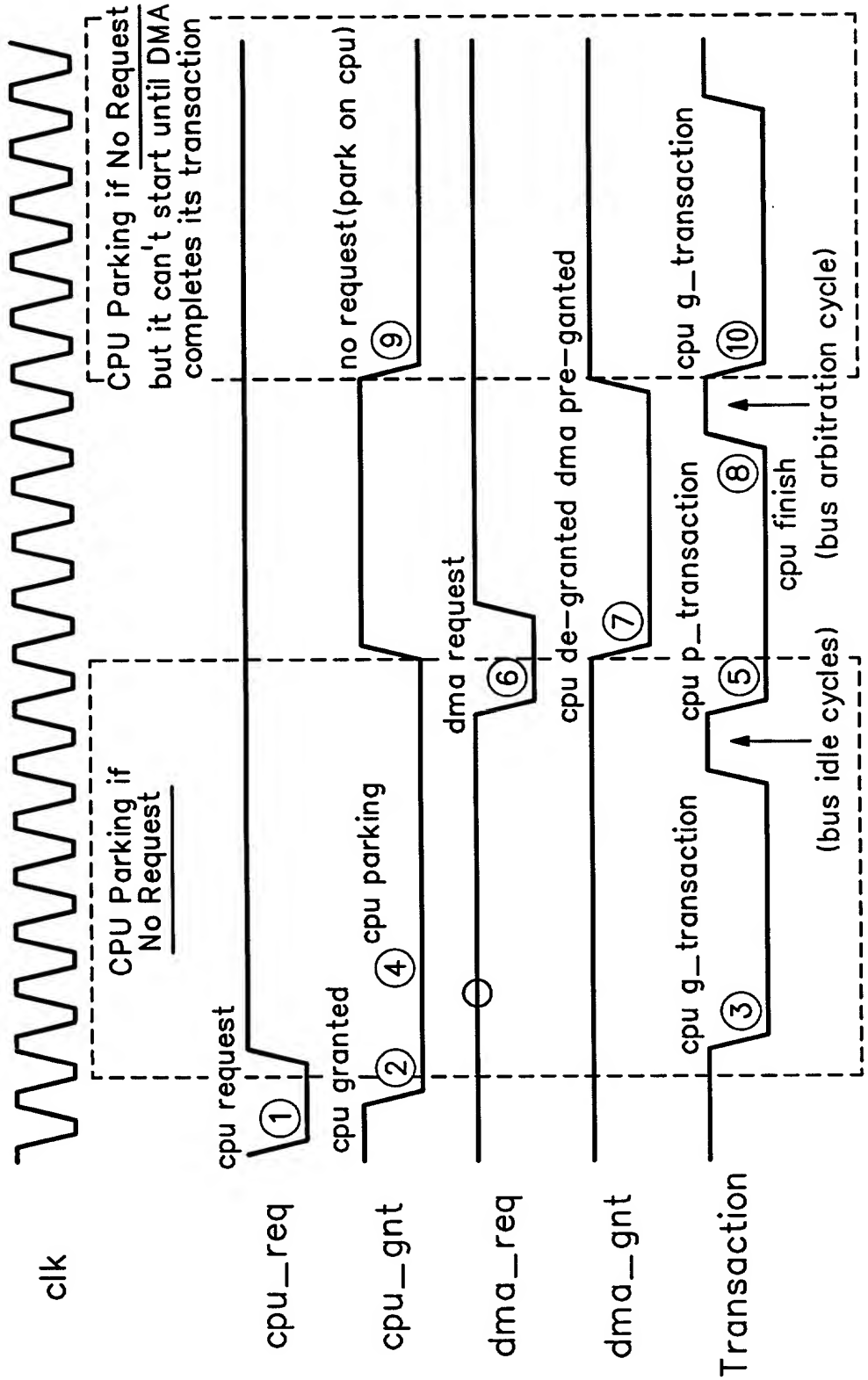

FIG.8

ARBITRATION PROTOCOL EXAMPLE
PARKING

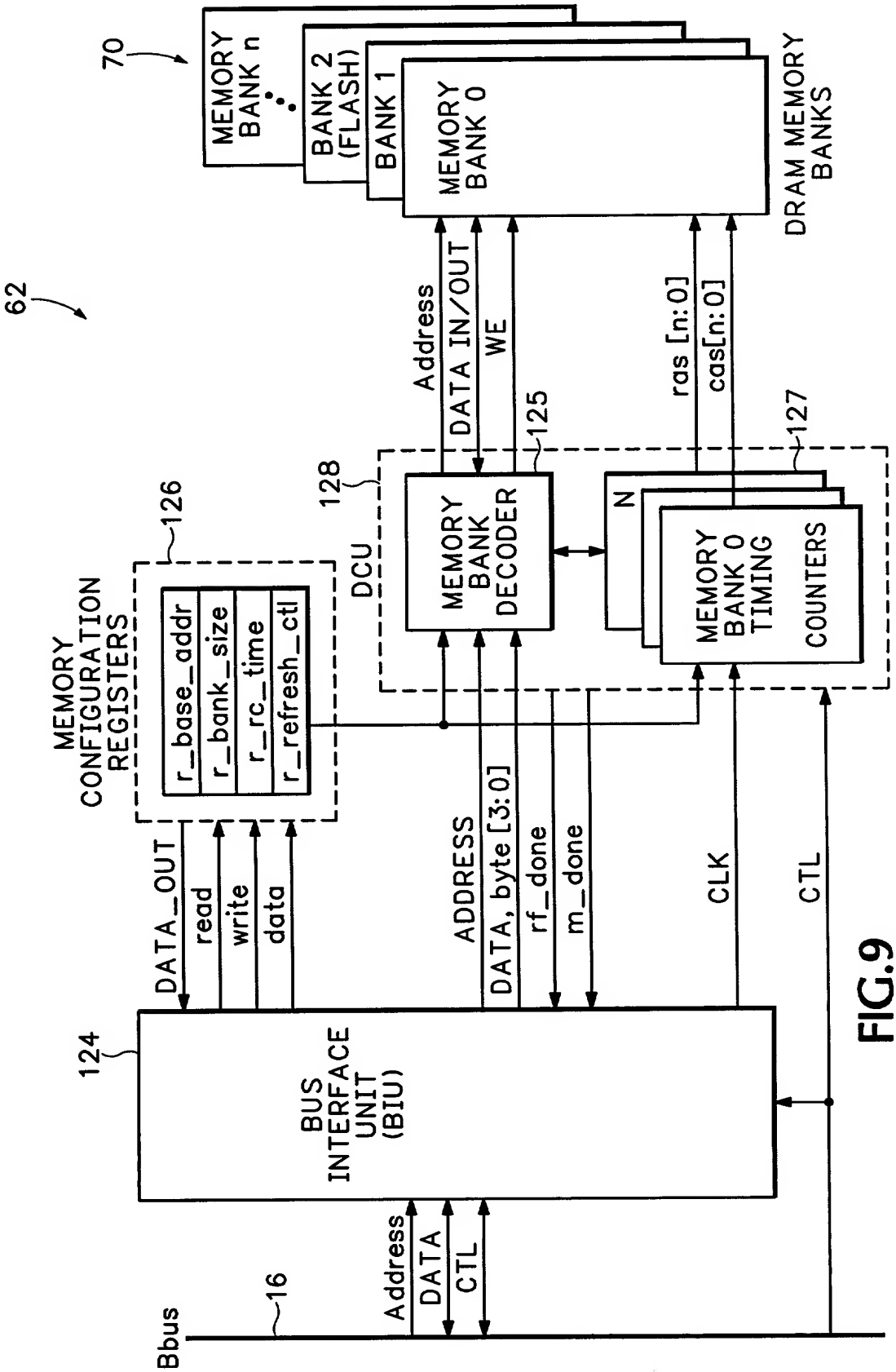

FIG.9
DRAM CONTROLLER

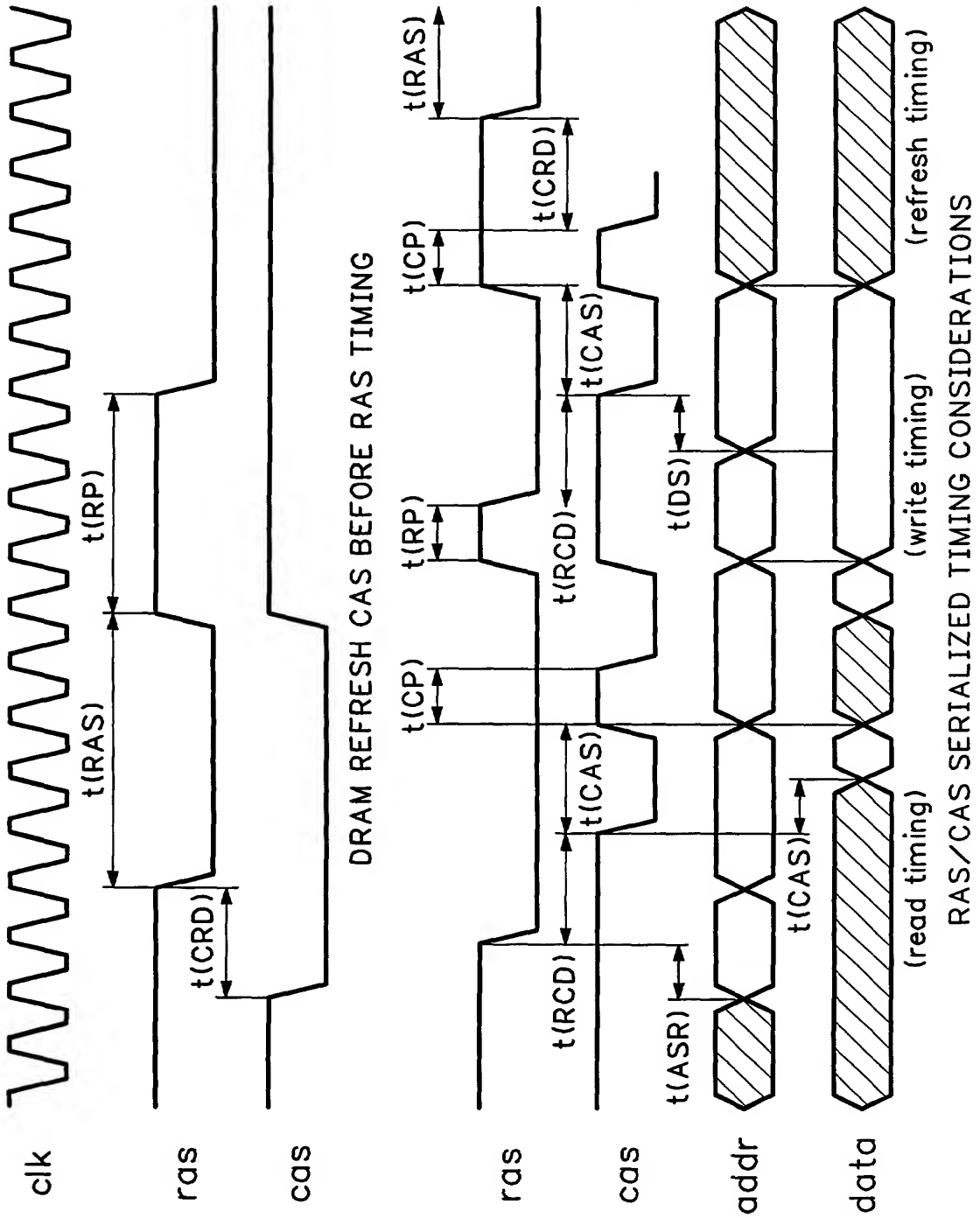
clk
ras
cas
t(RAS)
t(RP)
t(CRD)
DRAM REFRESH CAS BEFORE RAS TIMING
ras
cas
addr
data
t(RAS)
t(CRD)
t(CP)
t(CAS)
t(RP)
t(RCD)
t(DS)
t(CP)
t(CAS)
t(RCD)
t(ASR)
t(CAS)
(refresh timing)
(write timing)
(read timing)
RAS/CAS SERIALIZED TIMING CONSIDERATIONS

FIG.10

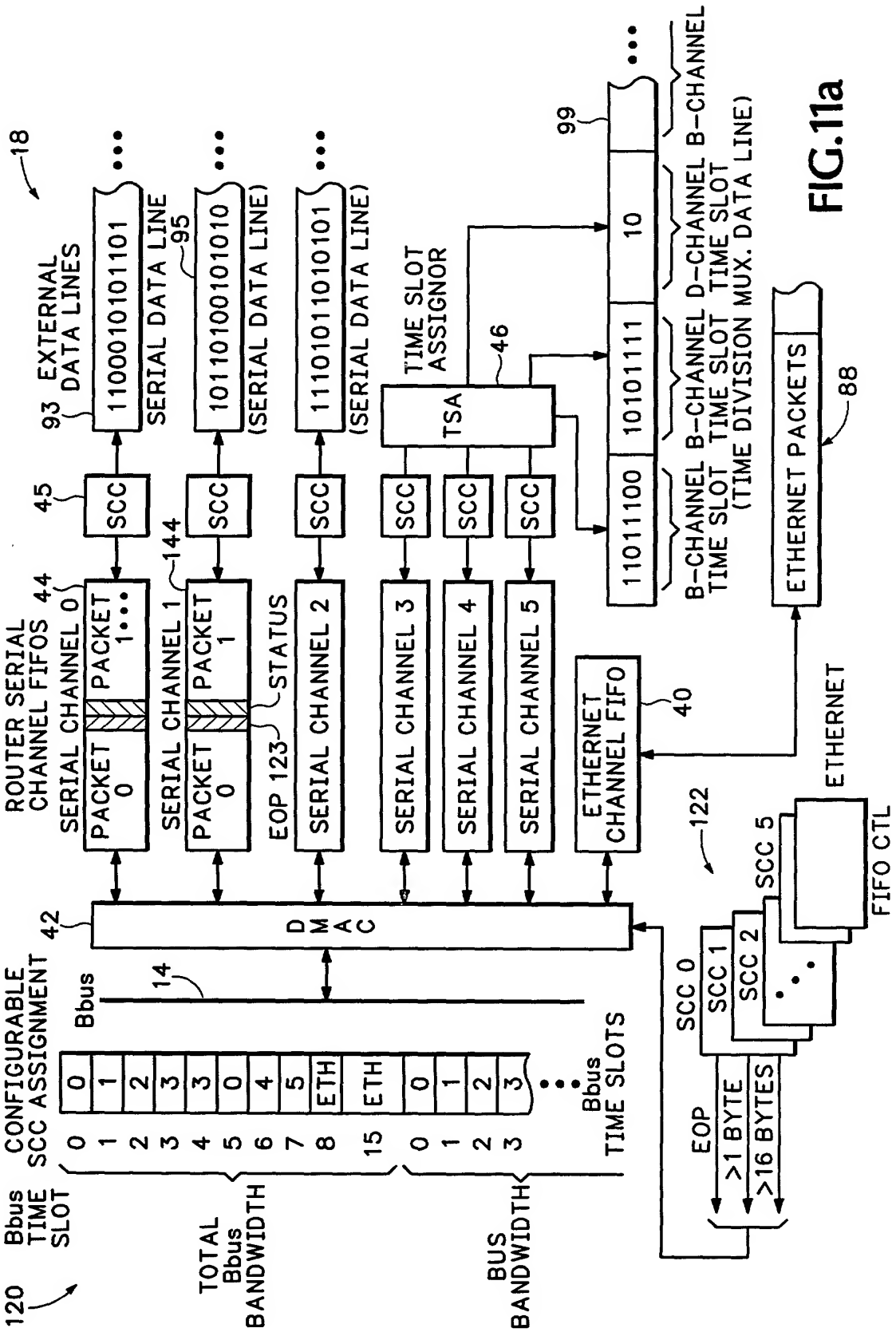
18
93 EXTERNAL DATA LINES
SERIAL DATA LINE 95
(SERIAL DATA LINE)
(SERIAL DATA LINE)
99
TIME SLOT ASSIGNOR
TSA
46
B-CHANNEL B-CHANNEL D-CHANNEL B-CHANNEL
TIME SLOT TIME SLOT TIME SLOT
(TIME DIVISION MUX. DATA LINE)
ETHERNET PACKETS
88
ROUTER SERIAL CHANNEL FIFOS 44
SERIAL CHANNEL 0
SERIAL CHANNEL 1
144
PACKET 0
PACKET 1
STATUS
EOP 123
SERIAL CHANNEL 2
SERIAL CHANNEL 3
SERIAL CHANNEL 4
SERIAL CHANNEL 5
ETHERNET CHANNEL FIFO
40
ETHERNET
45
SCC
42
DMAC
14
Bbus
CONFIGURABLE SCC ASSIGNMENT
Bbus TIME SLOT
120
TOTAL Bbus BANDWIDTH
BUS BANDWIDTH
Bbus TIME SLOTS
122
SCC 0
SCC 1
SCC 2
SCC 5
FIFO CTL
EOP
>1 BYTE
>16 BYTES

FIG.11a

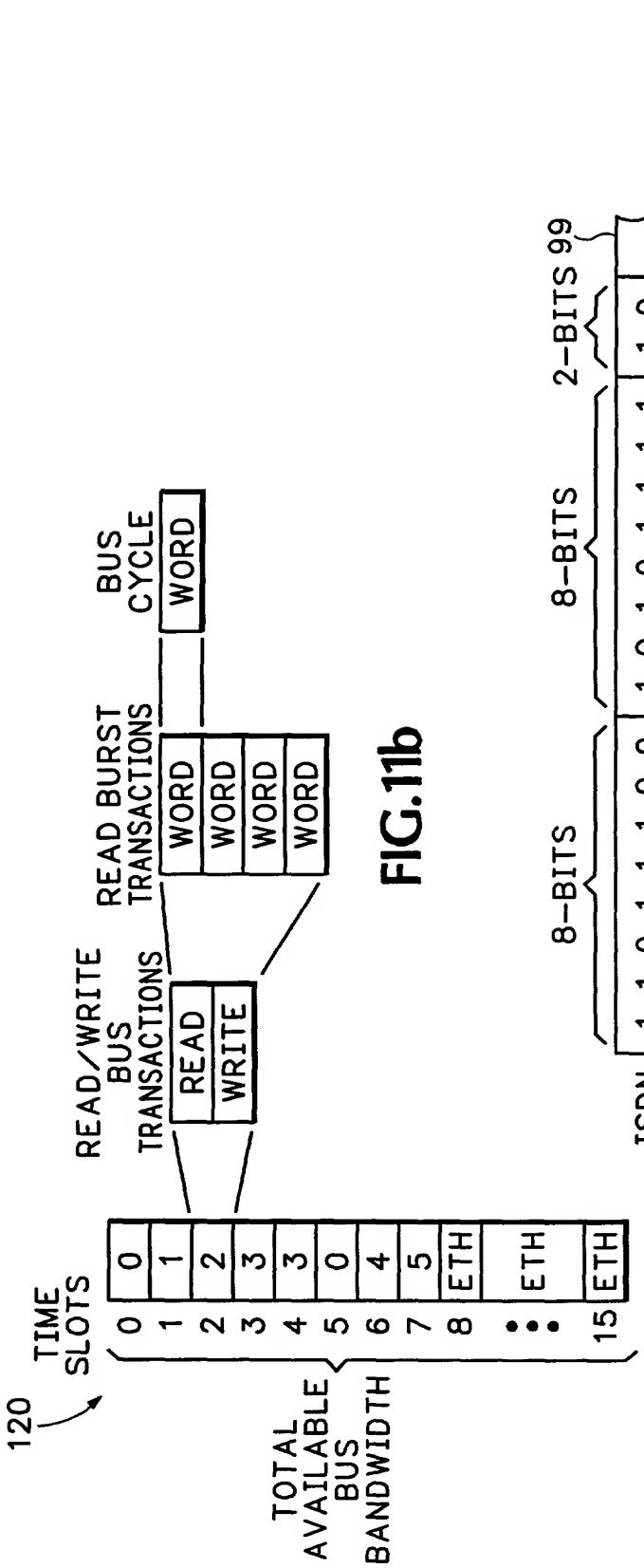

FIG.11b

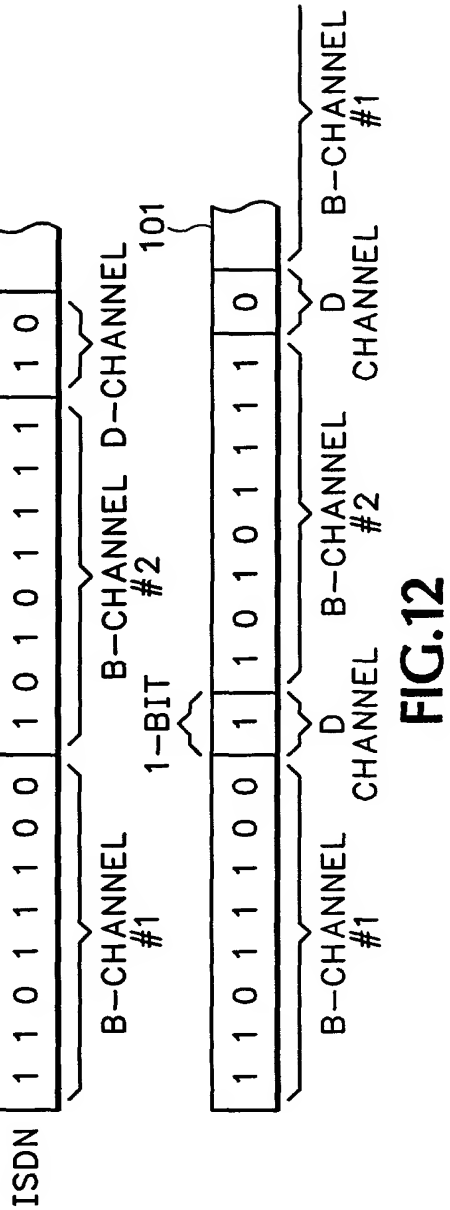

FIG.12

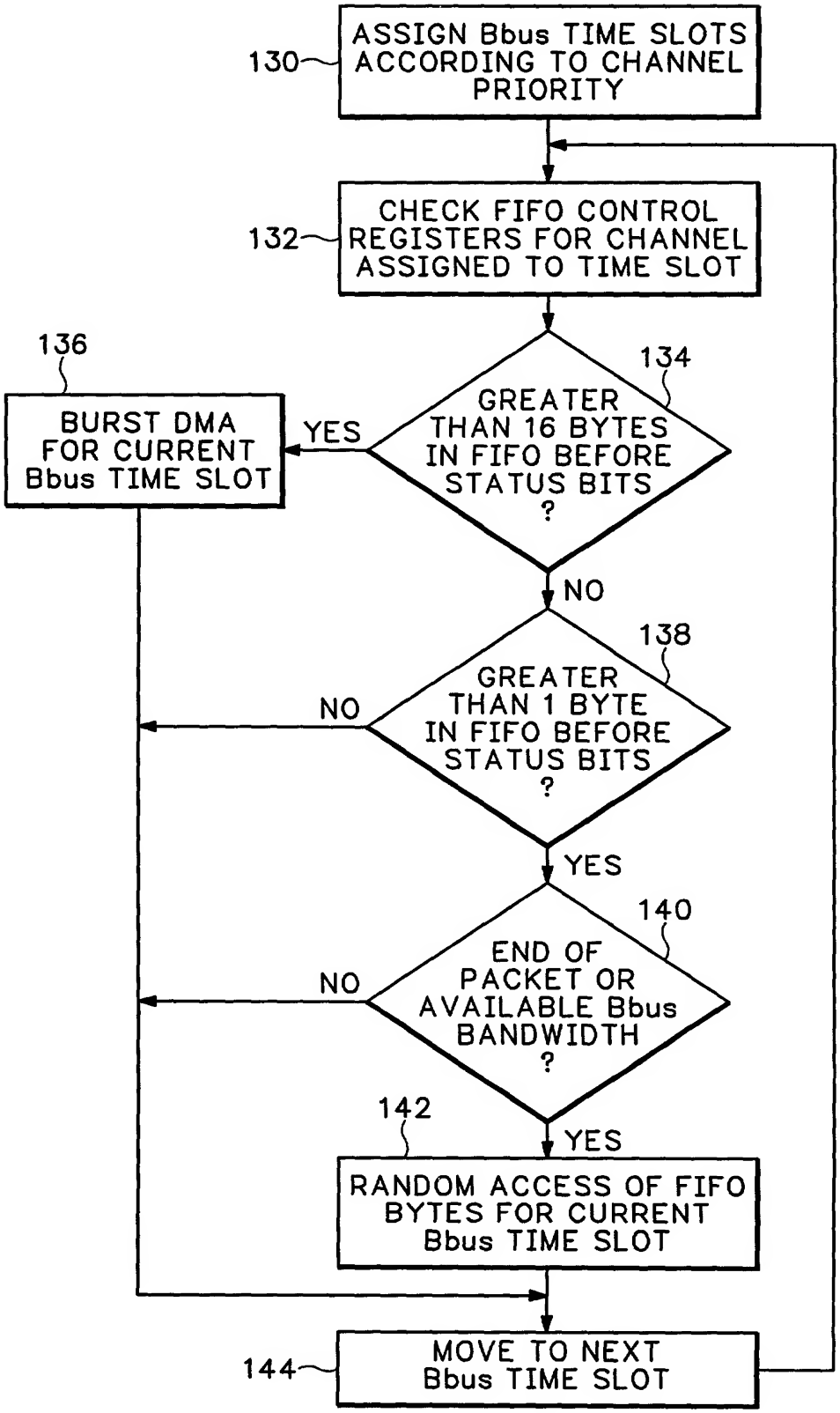
ASSIGN Bbus TIME SLOTS ACCORDING TO CHANNEL PRIORITY
130
CHECK FIFO CONTROL REGISTERS FOR CHANNEL ASSIGNED TO TIME SLOT
132
GREATER THAN 16 BYTES IN FIFO BEFORE STATUS BITS ?
134
YES
BURST DMA FOR CURRENT Bbus TIME SLOT
136
NO
GREATER THAN 1 BYTE IN FIFO BEFORE STATUS BITS ?
138
NO
YES
END OF PACKET OR AVAILABLE Bbus BANDWIDTH ?
140
NO
YES
RANDOM ACCESS OF FIFO BYTES FOR CURRENT Bbus TIME SLOT
142
MOVE TO NEXT Bbus TIME SLOT
144

FIG.13

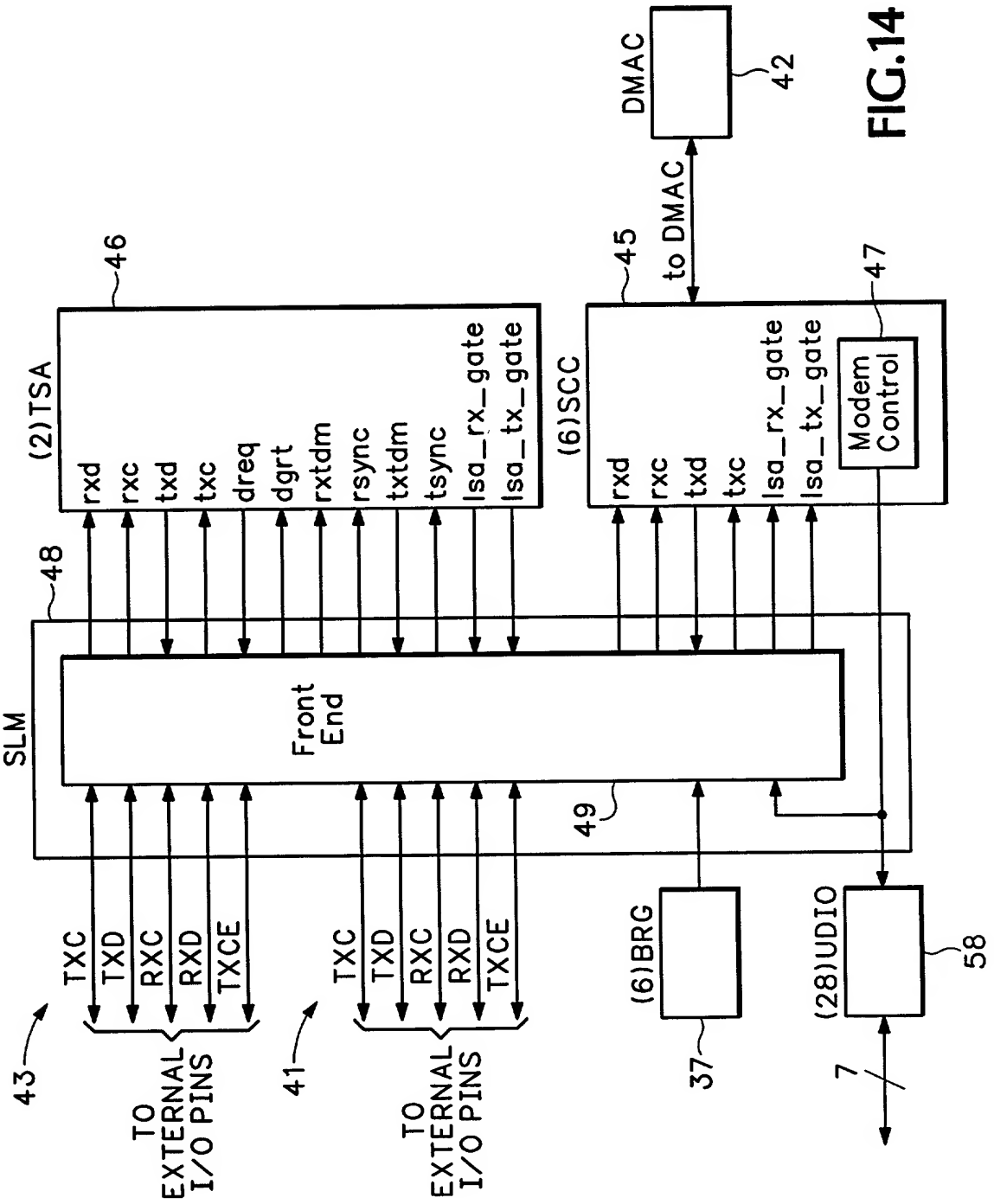
DMAC
42
to DMAC
45
47
46
(2)TSA
(6)SCC
Modem Control
rxd
rxc
txd
txc
dreq
dgrt
rxtdm
rsync
txtdm
tsync
lsa_rx_gate
lsa_tx_gate
48
SLM
Front End
49
TXC
TXD
RXC
RXD
TXCE
43
41
TO EXTERNAL I/O PINS
(6)BRG
37
(28)UDIO
58
7

FIG.14

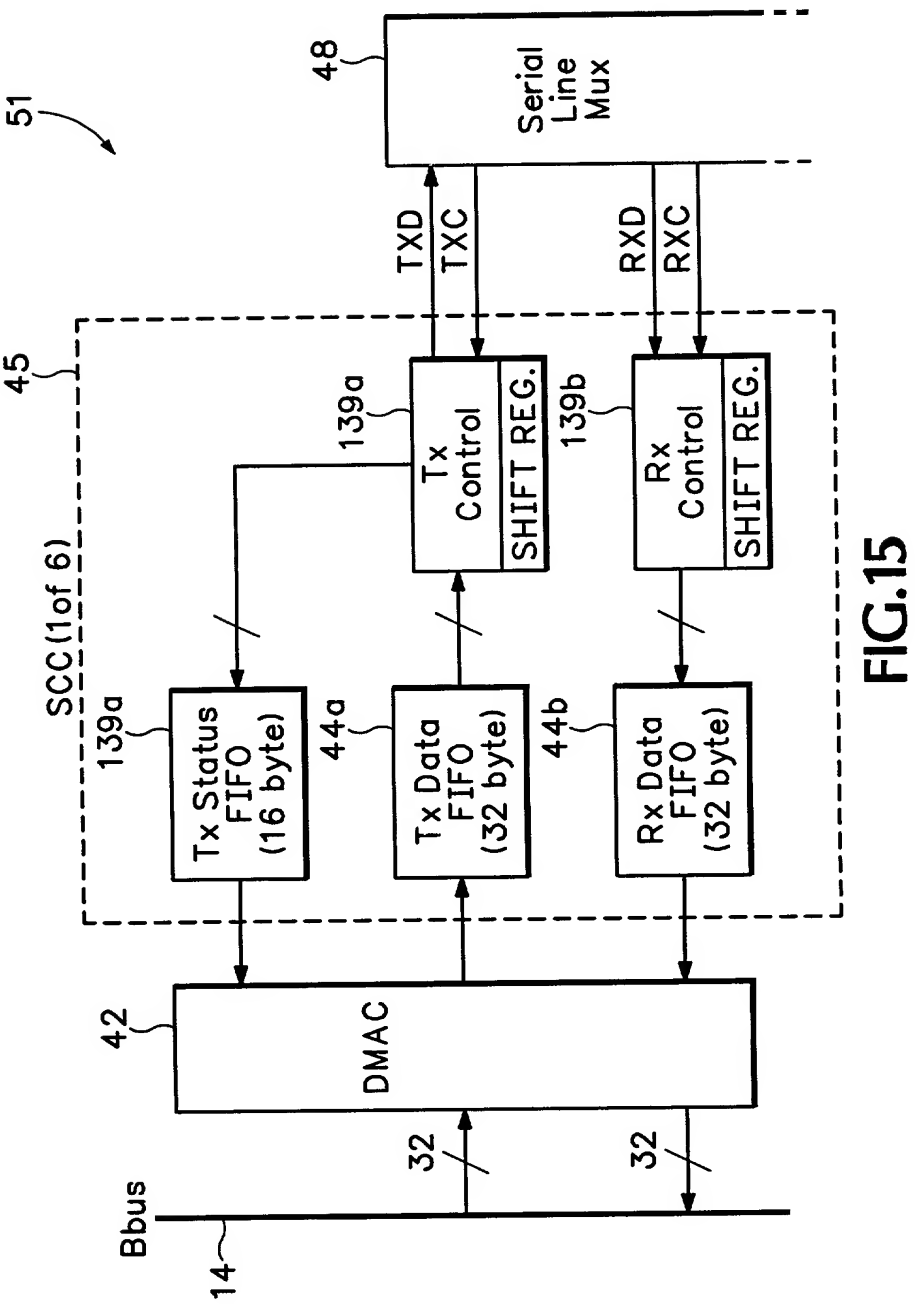
51
48
Serial Line Mux
TXD
TXC
RXD
RXC
45
SCC(1of 6)
139a
Tx Control
SHIFT REG.
139b
Rx Control
SHIFT REG.
139a
Tx Status FIFO (16 byte)
44a
Tx Data FIFO (32 byte)
44b
Rx Data FIFO (32 byte)
42
DMAC
32
32
Bbus
14

FIG.15

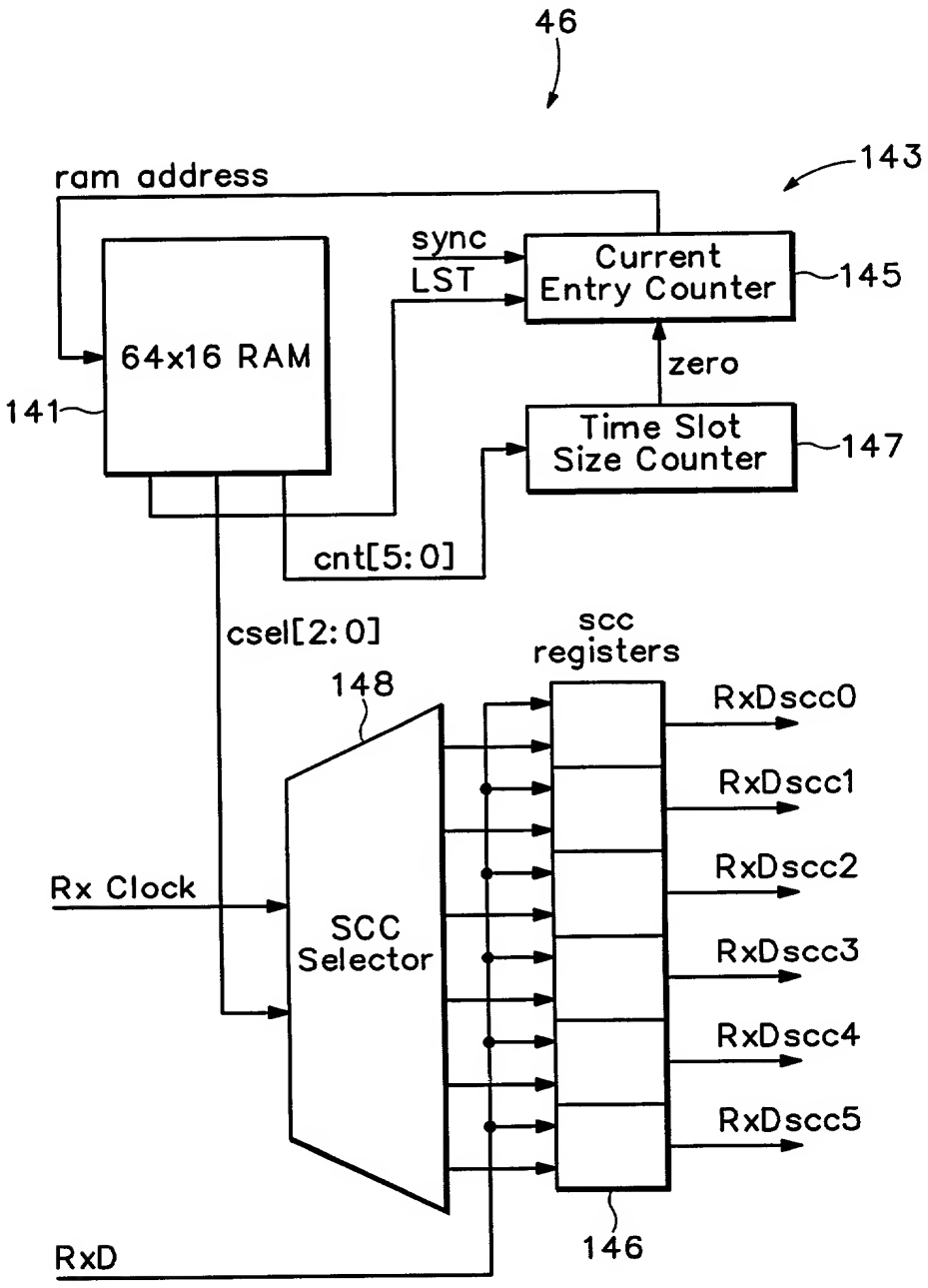

FIG.16
TSA RECEIVE
BLOCK DIAGRAM

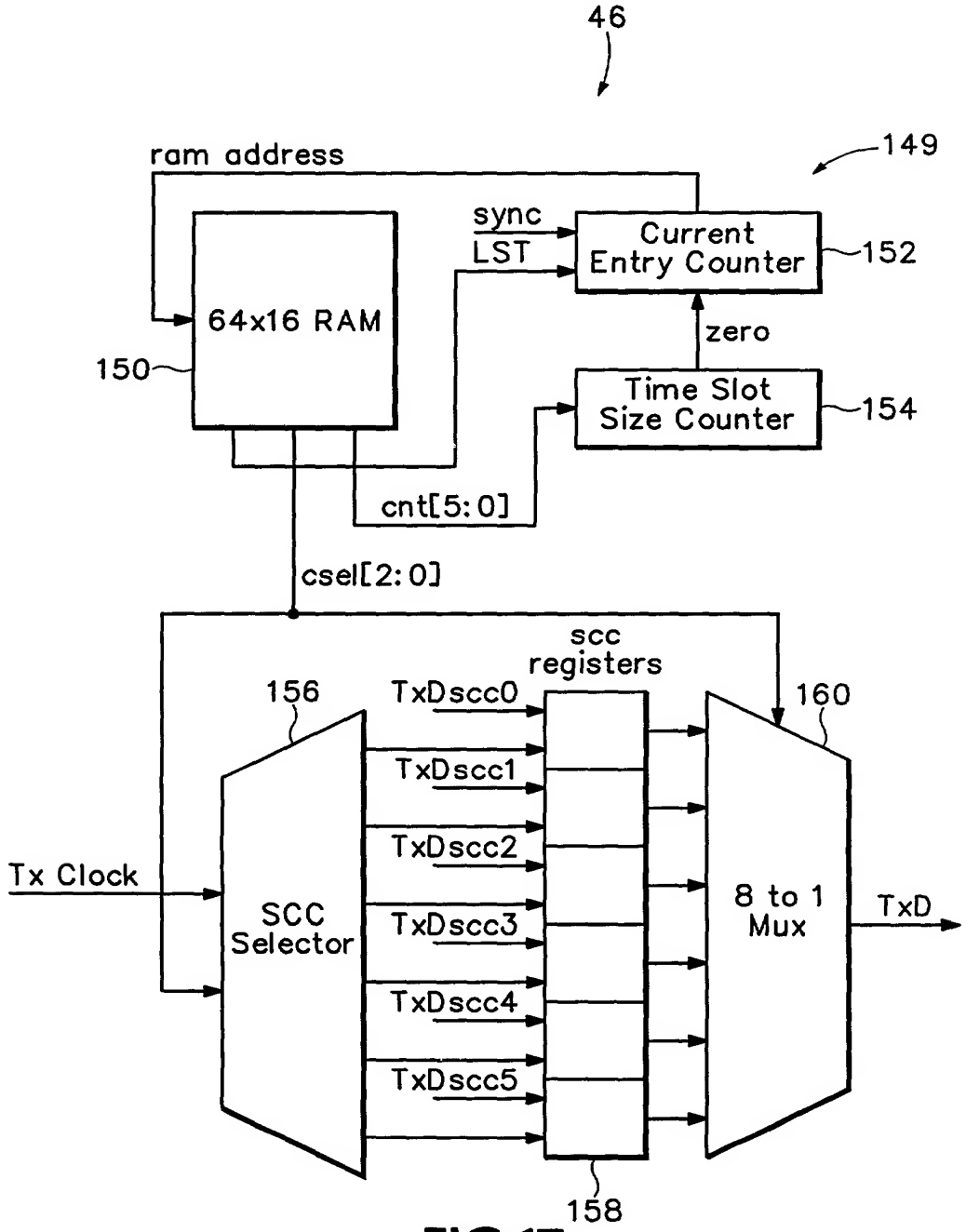

FIG.17
TSA TRANSMIT
BLOCK DIAGRAM

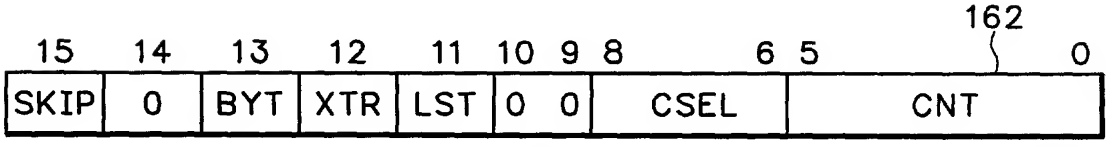

FIG.18

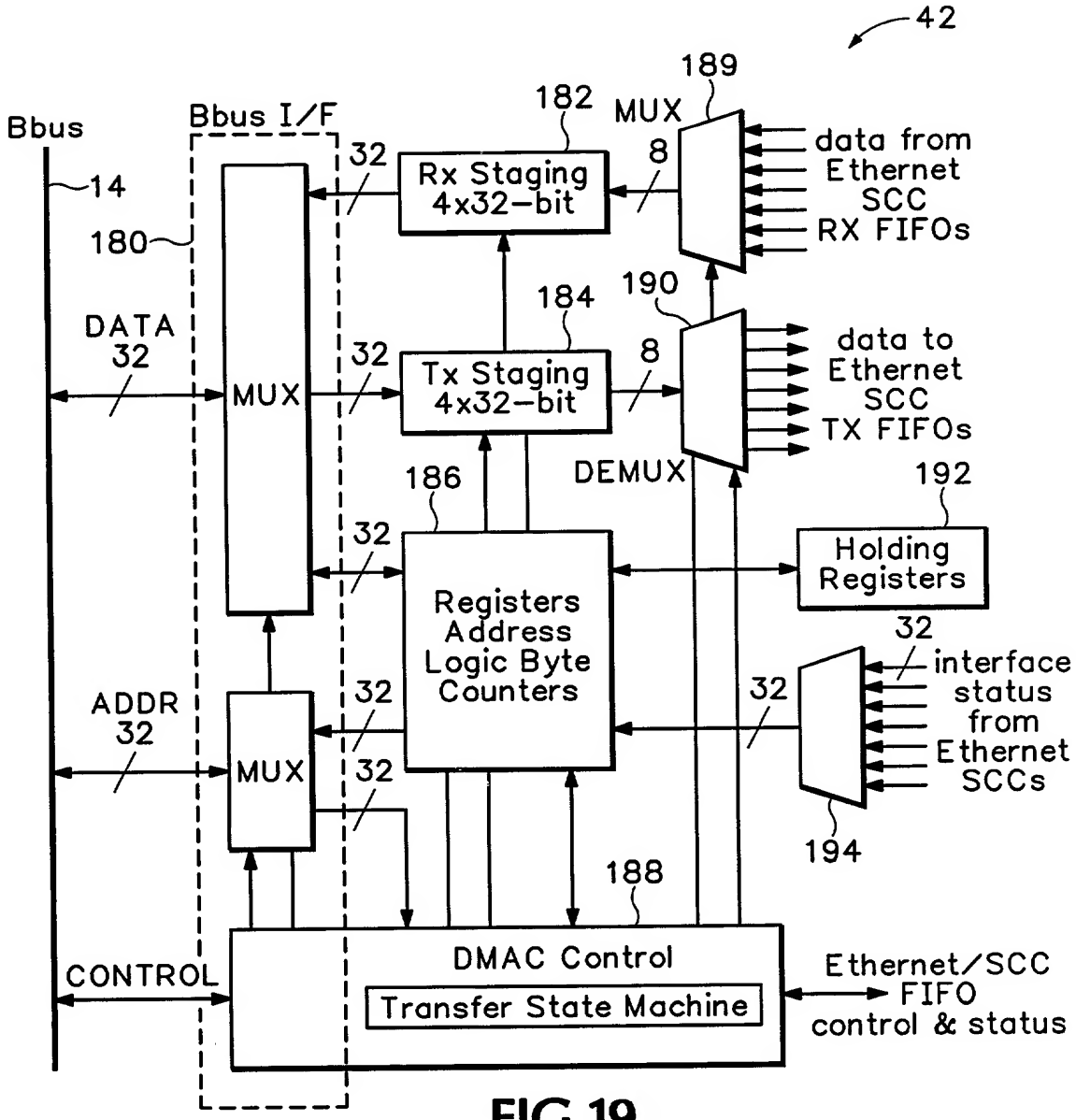

FIG.19

DMAC BLOCK DIAGRAM

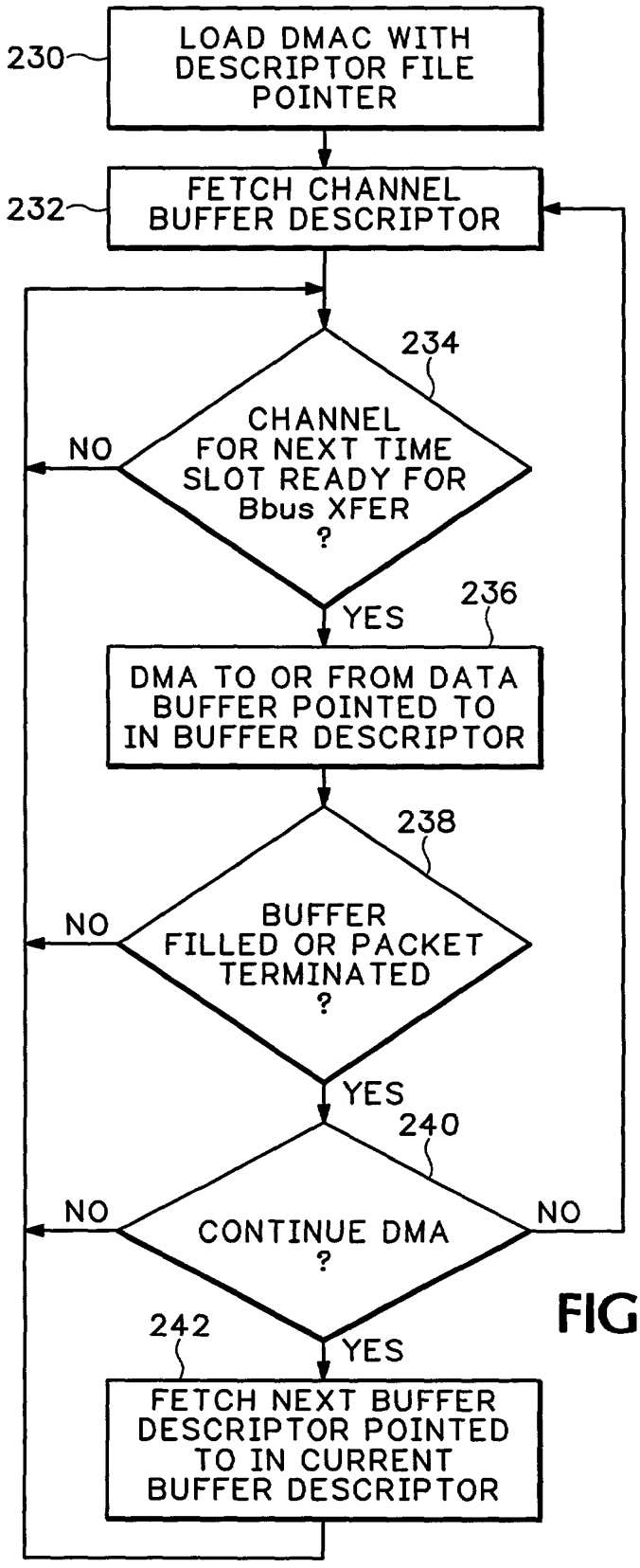
230
LOAD DMAC WITH DESCRIPTOR FILE POINTER
232
FETCH CHANNEL BUFFER DESCRIPTOR
234
CHANNEL FOR NEXT TIME SLOT READY FOR Bbus XFER ?
NO
YES
236
DMA TO OR FROM DATA BUFFER POINTED TO IN BUFFER DESCRIPTOR
238
BUFFER FILLED OR PACKET TERMINATED ?
NO
YES
240
CONTINUE DMA ?
NO
NO
YES
242
FETCH NEXT BUFFER DESCRIPTOR POINTED TO IN CURRENT BUFFER DESCRIPTOR

FIG.20

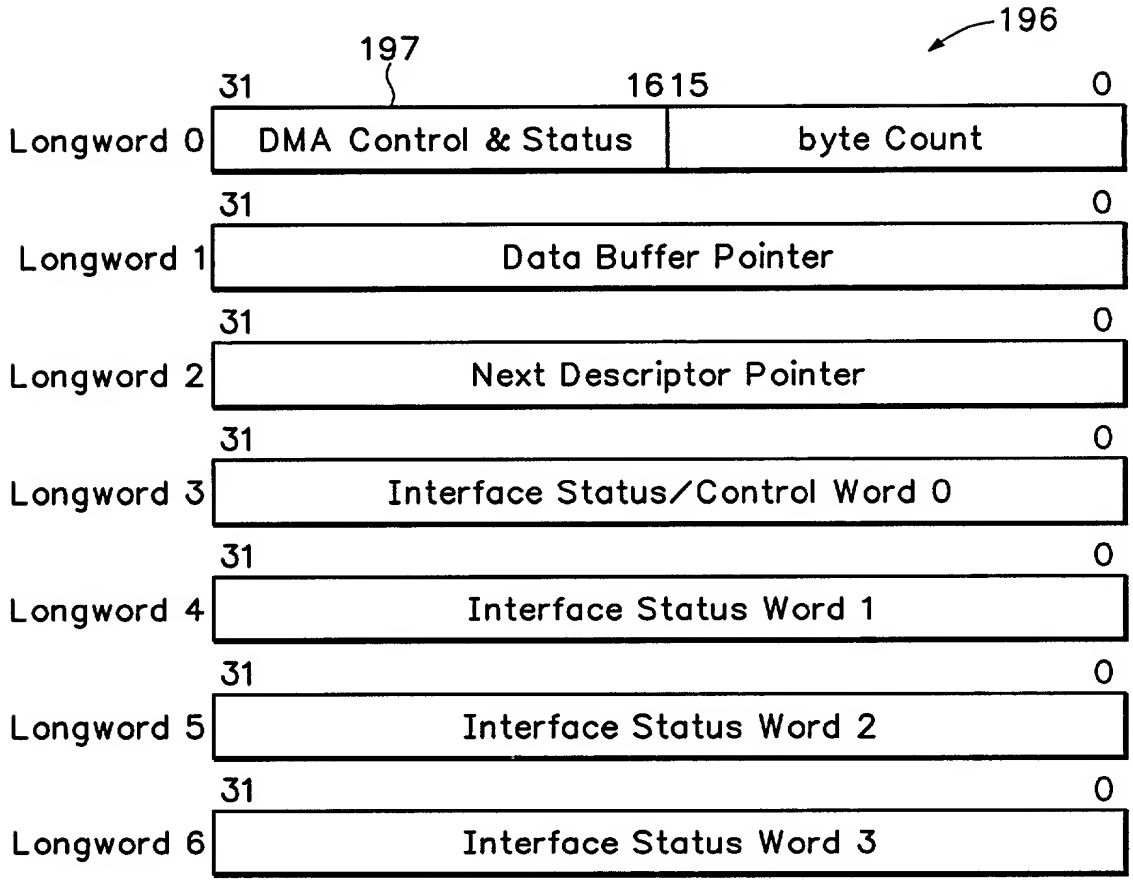

FIG.21
BUFFER DESCRIPTOR

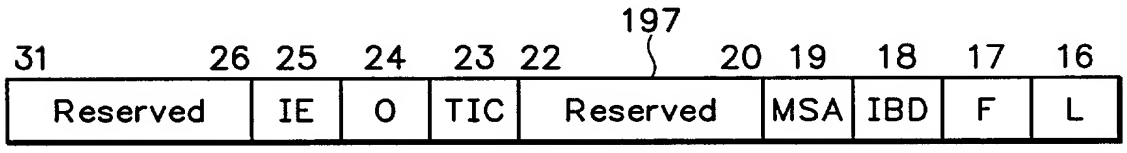

FIG.22
DMA CONTROL & STATUS
FIELD OF DESCRIPTOR

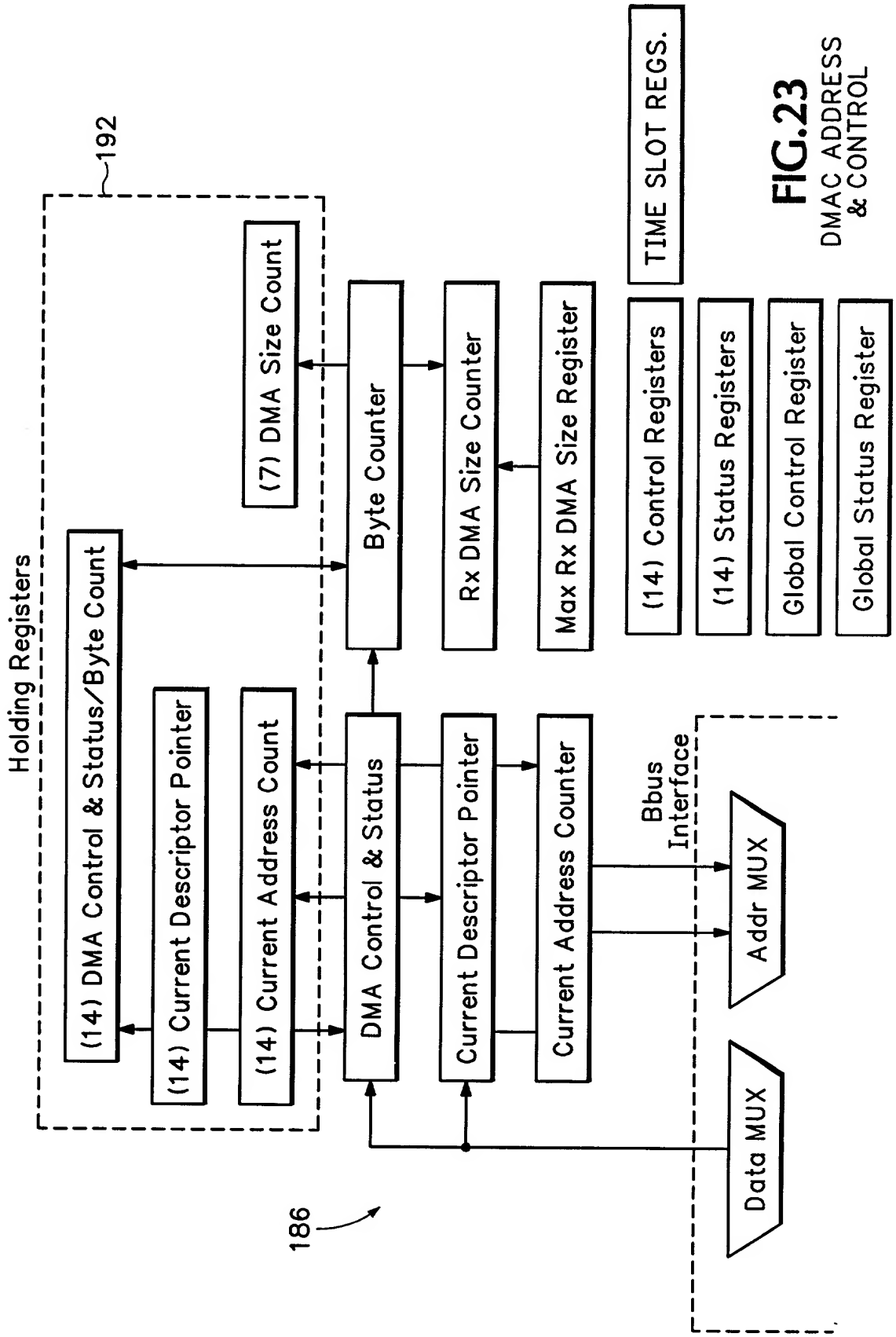

FIG.23
DMAC ADDRESS & CONTROL

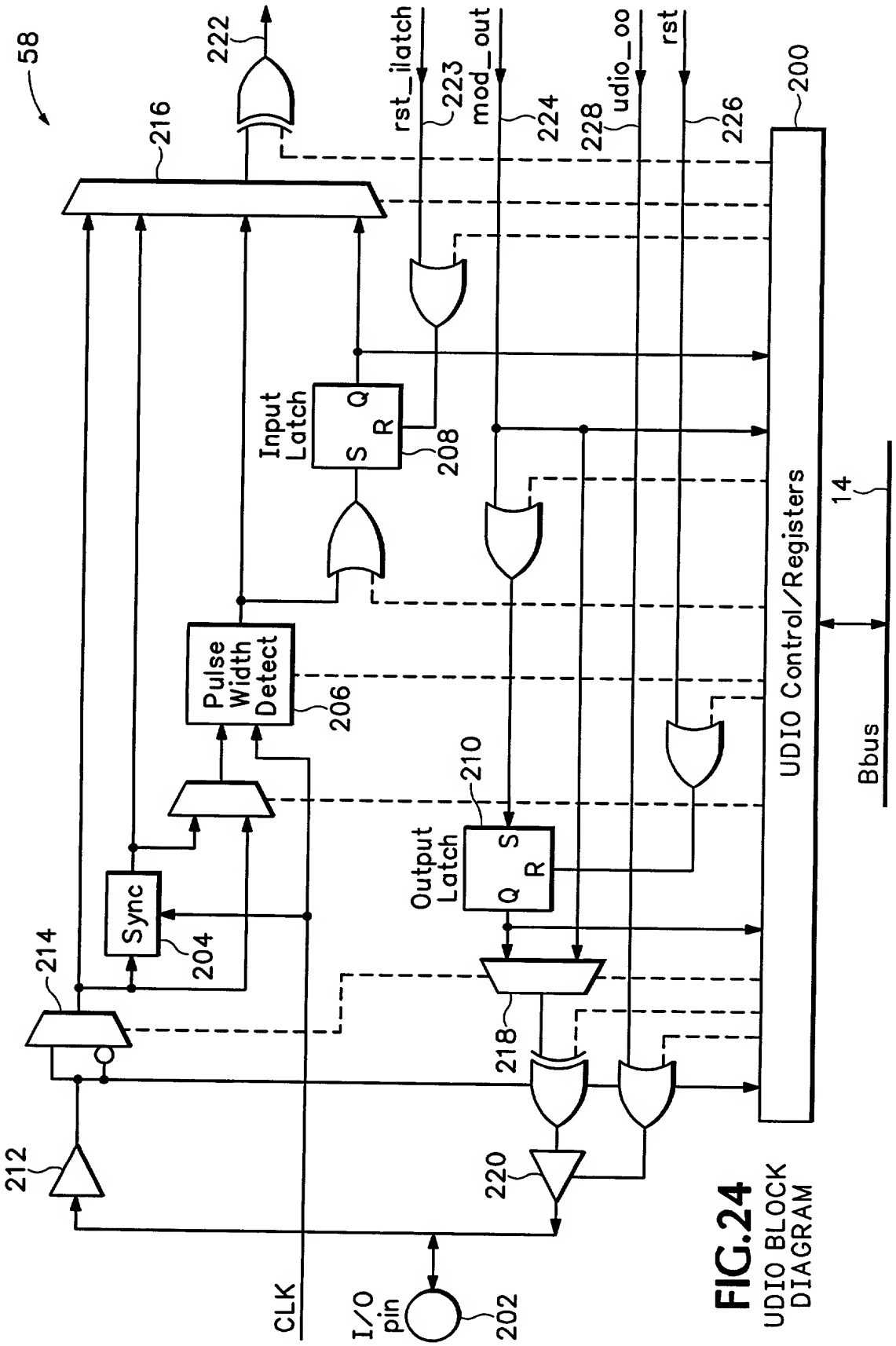

FIG.24
UDIO BLOCK DIAGRAM

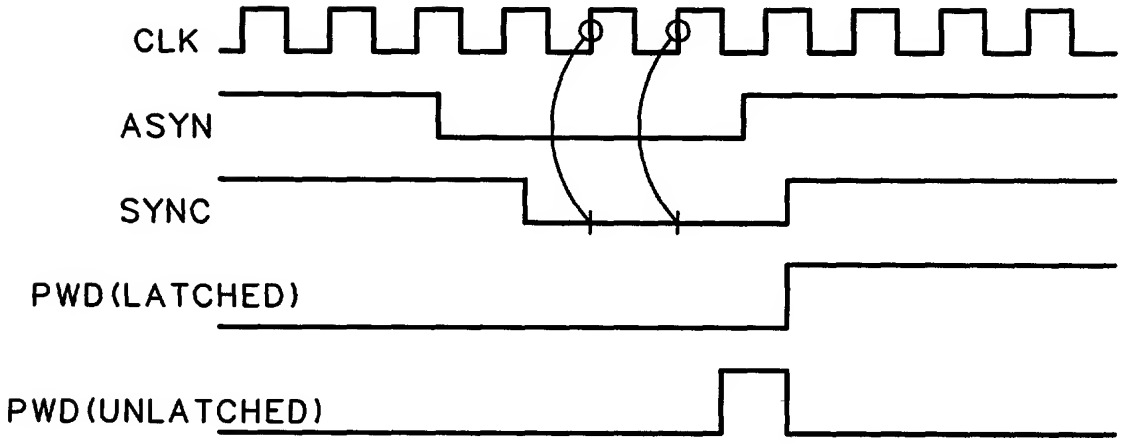
CLK
ASYN
SYNC
PWD(LATCHED)
PWD(UNLATCHED)

FIG.25

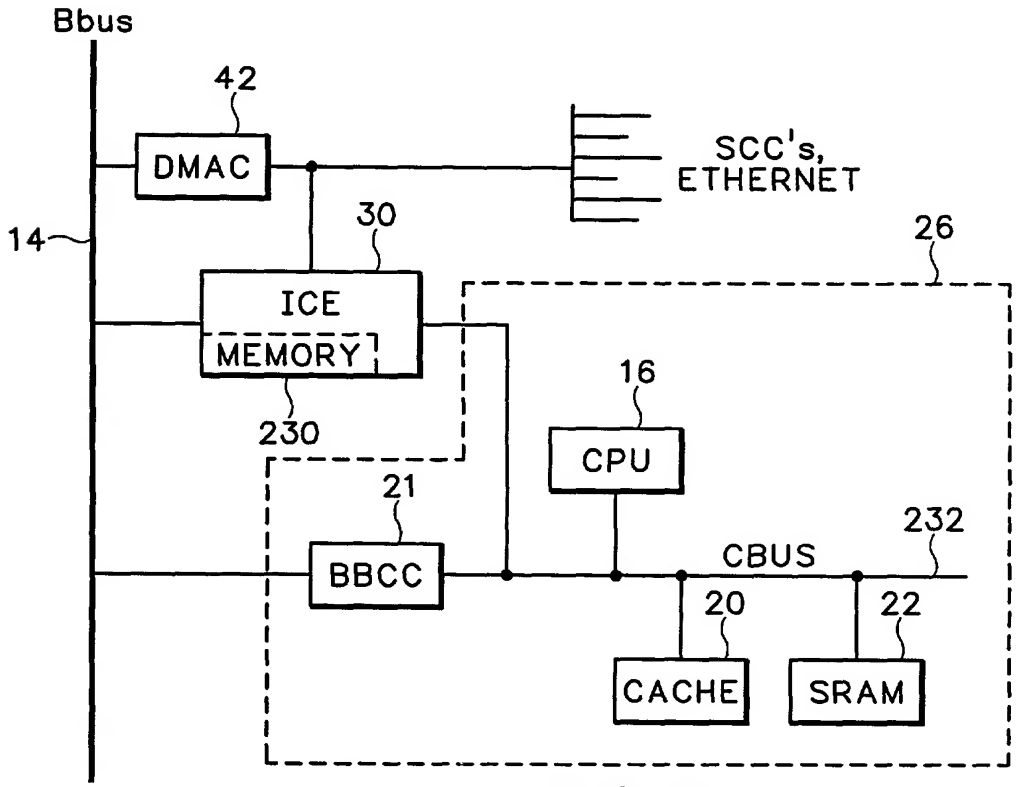
Bbus
42
DMAC
SCC's,
ETHERNET
14
30
26
ICE
MEMORY
230
16
CPU
21
232
BBCC
CBUS
20
22
CACHE
SRAM

FIG.26

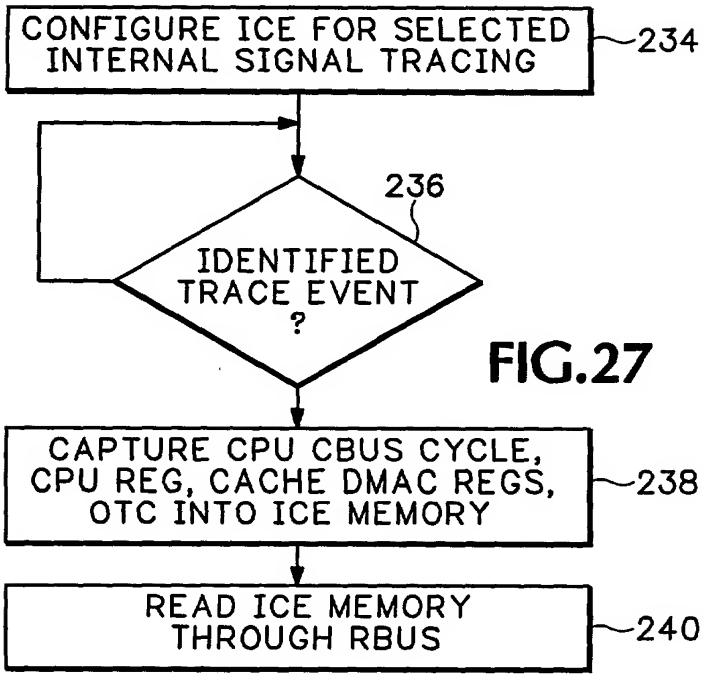
CONFIGURE ICE FOR SELECTED INTERNAL SIGNAL TRACING
234
236
IDENTIFIED TRACE EVENT ?
CAPTURE CPU CBUS CYCLE, CPU REG, CACHE DMAC REGS, OTC INTO ICE MEMORY
238
READ ICE MEMORY THROUGH RBUS
240

FIG.27

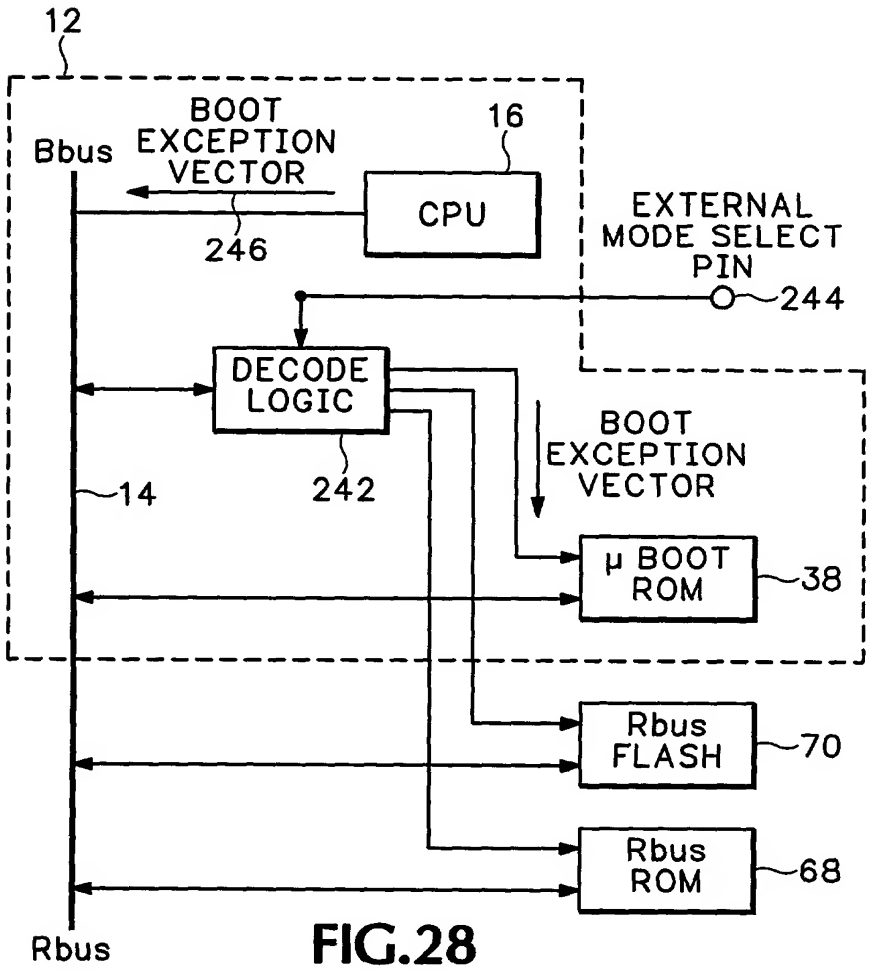
12
BOOT EXCEPTION VECTOR
16
Bbus
CPU
246
EXTERNAL MODE SELECT PIN
244
DECODE LOGIC
242
BOOT EXCEPTION VECTOR
14
μ BOOT ROM
38
Rbus FLASH
70
Rbus ROM
68
Rbus

FIG.28

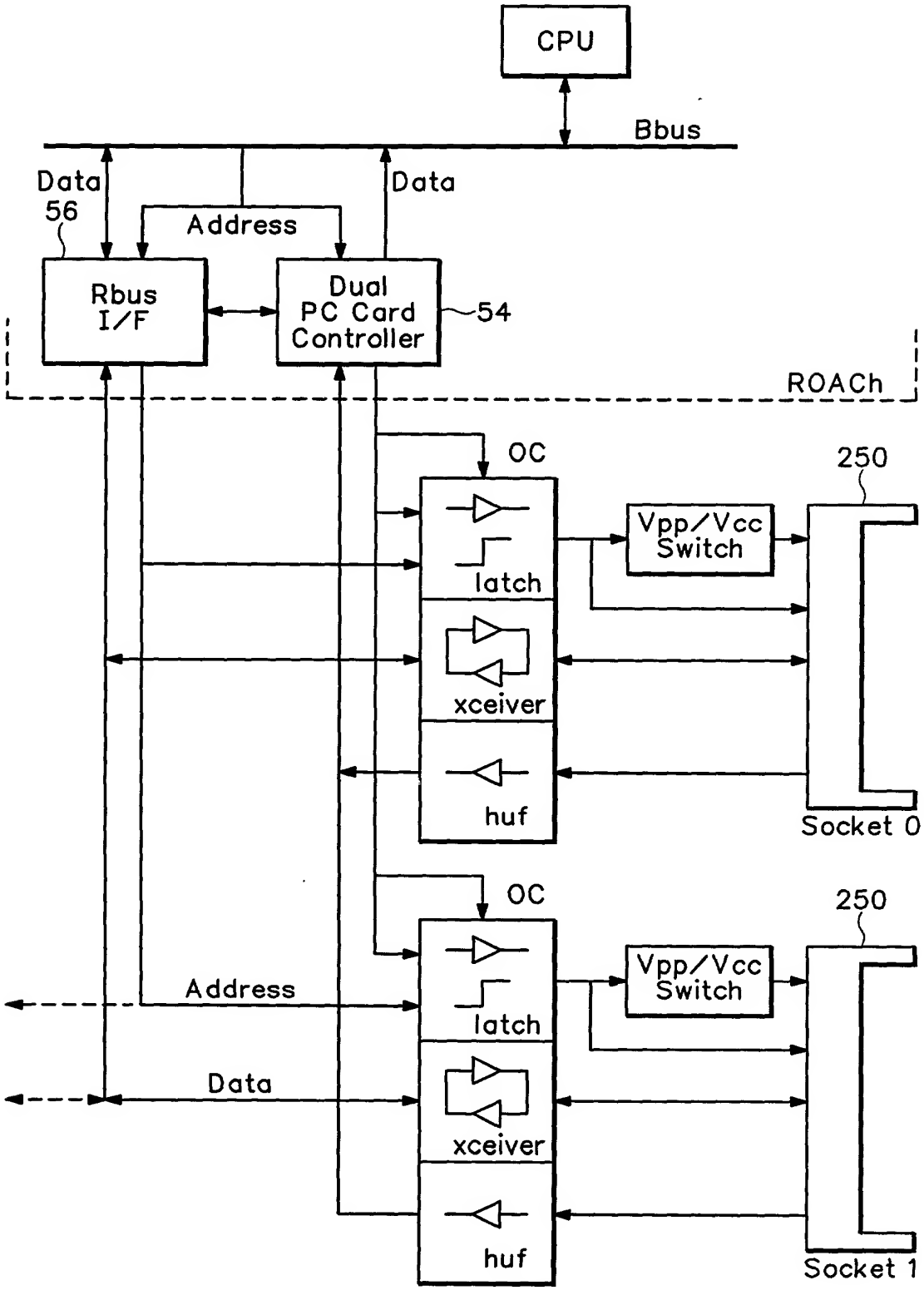

FIG.29
PC CARD INTERFACE